In The Claims

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19 (Original): A double data rate compatible input/output (I/O) element circuit for an I/O terminal of a logic array comprising:

a first output register having an input for receiving a first output signal from the logic array and an output for registering the first output signal upon a first edge in an output clock signal,

a second output register having an input for, in at least one mode of operation, receiving a second output signal from the logic array and an output for registering the second output signal upon the first edge in the output clock signal,

a multiplexer having a first input connected to the output of the first output register, a second input connected to the output of the second output register, an address input configurable to receive the output clock signal, and an output connectable to the I/O terminal.

20 (Original): The I/O element circuit of claim 19 wherein the first output register is a delay type flip flop circuit and the second output register is a delay type latch circuit.

21 (Original): The I/O element circuit of claim 19 wherein the address input of the multiplexer in the output block circuit is configurable to receive either the output clock signal or a fixed address signal corresponding to a multiplexer input address for the registered first output signal.

22 (Original): The I/O element circuit of claim 19 wherein both programmably delayed and non-delayed versions of the signal output by the multiplexer are connectable to the I/O terminal.

23 (Original): A first double data rate compatible input/output (I/O) element circuit for a first I/O terminal of a logic array and a second double data rate compatible input/output (I/O) element circuit for a second I/O terminal of the logic array, wherein:

the first I/O element circuit comprises

a first input register having an input for receiving a signal at the first I/O terminal and an output for registering the first I/O terminal signal upon a first edge in

an input clock signal, the output of the first input register being connectable to the logic array, and

a second input register having an input for receiving the first I/O terminal signal and an output for registering the first I/O terminal signal upon a second edge in the input clock signal, the output of the second input register being couplable to the logic array;

and the second I/O element circuit comprises

a first output register having an input for receiving a first output signal from the logic array and an output for registering the first output signal upon a first edge in an output clock signal,

a second output register having an input for, in at least one mode of operation, receiving a second output signal from the logic array and an output for registering the second output signal upon the first edge in the output clock signal,

a multiplexer having a first input connected to the output of the first output register, a second input connected to the output of the second output register, an address input configurable to receive the output clock signal, and an output connectable to the second I/O terminal.

24 (Original): The I/O element circuits of claim 23 wherein the input block circuit further comprises an input bistable circuit having an input for receiving the registered first I/O terminal signal output by the second input register and an output for latching the registered first I/O terminal signal upon the first edge in the input clock signal, the output of the input bistable circuit being connectable to the logic array.

25 (Original): The I/O element circuits of claim 24 wherein the first input register, the second input register, and the first output register are delay type flip flop circuits, and wherein the second output register and the input bistable circuit are delay type latch circuits.

26 (Original): The I/O element circuits of claim 24 wherein the input clock signal and output clock signal are provided by different clock sources.

27 (Original): A programmable input/output (I/O) element circuit for a bidirectional I/O terminal of a logic array comprising:

an input register having an input for receiving a signal at the I/O terminal and an output for registering the I/O terminal signal upon a first edge in an input clock signal, the output of the first input register being connectable to the logic array;

an output register having an input for receiving an output signal from the logic array and an output for registering the output signal upon a first edge in an output clock signal, the registered output signal being connectable to the I/O terminal via a gated output buffer; and

an output enable circuit for receiving an enable signal from the logic array and providing an output enable signal to a gating input of the gated output buffer via a programmable delay circuit, wherein the output enable signal provides a slower turn-on time than turn-off time for the gated output buffer.

28 (Original): The I/O element circuit of claim 27 wherein the programmable delay circuit comprises a logic gate having first and second inputs and an output, the first logic gate input receiving a signal input to the programmable delay circuit, the second logic gate input receiving a delayed version of the signal input to the programmable delay circuit, and the output of the logic gate providing the output enable signal.

29 (Original): The I/O element circuit of claim 28 wherein the output enable signal enables the gated output buffer when high and wherein the logic gate in the programmable delay circuit comprises an AND gate.

30 (Original): The I/O element circuit of claim 28 wherein the output enable signal enables the gated output buffer when low and wherein the logic gate in the programmable delay circuit comprises an OR gate.

31 (Original): The I/O element circuit of claim 28 wherein the output enable circuit comprises an output enable register having an input for receiving the enable signal from the logic array and an output for providing a registered enable signal upon the first edge in the output clock signal, the registered enable signal being provided as the input to the programmable delay circuit.